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10/764,513	01/27/2004	Hidenori Nanki	56937-108	9962

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EXAMINER	
KROPCHECK, MICHAEL C	
ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,513	NANKI ET AL.	
	Examiner	Art Unit	
	MICHAEL C. KROFCHECK	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-5 and 11-13* is/are allowed.

6)☒ Claim(s) *6-10, 14-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the RCE filed on 3/14/2008.

2. Claims 3-12, 14, 16, 18, and 20 have been amended.

3. The objections/rejections not restated herein have been withdrawn.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 6-10, 14-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. With respect to claims 7-8 each claim includes a built-in RAM and an interrupt saved information unit that have "a secure bit" which is used to hold "one or more secure bits." However, if there is only one secure bit, how will they hold the possibly multiple secure bits? The examiner suggests indicating that the RAM and interrupt saved information unit have one or more secure bits if supported by the applicant's specification.

7. With respect to claims 6-8, 10 each claim includes a general purpose register that has "a secure bit" which is used to hold "one or more secure bits." However, if there is only one secure bit, how will it hold the possibly multiple secure bits? The

examiner suggests indicating that the GPR has one or more secure bits if supported by the applicant's specification.

8. With respect to claim 9, the claim indicates that the DMA has "a secure bit having a function of holding the one or more secure bits." However, if there is only one secure bit in the DMA, how will it hold the possibly multiple secure bits? The examiner suggests indicating that the DMA has one or more secure bits if supported by the applicant's specification.

9. Claims 20-21 recite the limitations "the mode" in each claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Ishimoto, US patent 6101586 and Koizumi, US patent 5414864.

14. With respect to claim 6, Abraham teaches of an information processing apparatus for accessing memory spaces including a user memory space and a secure memory space (fig. 1; item 105, 109), comprising: a secure bit generating unit for determining which of the user memory space and the secure memory space is indicated by address information (column 2, lines 57-67, as data is restricted from accessing a memory in either circumstance, it is abundantly clear to one of ordinary skill in the art that there is something that determines which memory the access is directed to through its address), and

delivering data with one or more secure bits into a general purpose register with a secure bit having a function of receiving and holding the data with one or more secure bits (fig. 1; column 2, lines 45-48; the Intel 80C186 processor inherently contains general purpose registers used for arithmetic operation and I/O operation. Intel's

"80C186EA/80C188EA Microprocessor User's Manual" provides support for this in sections 2.1, 2.1.3 on pages 2-1, 2-4 to 2-5);

a built-in memory space for receiving and holding the data with one or more secure bits from the general purpose register and delivering the data with one or more secure bits to the general purpose register (fig. 1; item 105, 109); and

a data output control unit having a function of controlling a data transfer to an external space by using the secure bit (column 2, lines 57-67);

wherein the data output control unit performs a control operation to determine whether the data transfer to the external space is prohibited or not by a value of the secure bits (column 2, lines 57-67; column 3, lines 10-12).

Abraham fails to explicitly teach of the built-in memory space being a RAM. However, Ishimoto teaches of the built-in memory space being a RAM (column 11, lines 46-49).

Abraham fails to explicitly teach of a value of the secure bits being set in the general purpose register. However, Koizumi teaches of a status value being set in the general purpose register (column 2, lines 36-42).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham and Ishimoto at the time of the invention to use RAM as the unprivileged memory in Abraham as taught in Ishimoto, since RAM is the most commonly available and most versatile type of memory.

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, and Koizumi at the time of the invention to indicate the privileged

and unprivileged states in the GPR of Abraham as taught in Koizumi so the status is directly accessible by the processor.

15. Claims 14-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Ishimoto, and Koizumi as applied to claim 6 above, and in further view of Guttag.

16. With respect to claim 14, Guttag teaches of wherein the data control unit determines whether the data transfer to the user memory space is prohibited or not irrespective of a mode associated with a CPU (column 2, lines 3-54).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi, and Guttag at the time of the invention to determine the allowability of data transfer independently of the CPU in the combination of Abraham, Ishimoto, Koizumi as taught in Guttag so that the protection of software is extended against numerous external peripheral devices (Guttag, column 1, lines 65-68).

17. With respect to claim 15, Abraham teaches of wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode (column 2, lines 57-61).

18. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Ishimoto, Koizumi and Banno.

19. With respect to claim 9, the combination of Abraham, Ishimoto, Koizumi teach of the limitations cited above with respect to claim 6.

Abraham fails to explicitly teach of a direct memory access unit with a secure bit having a function of holding the one or more secure bits. However, Banno teaches of a computer system including a direct memory access controller (column 1, lines 11-15).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi and Banno at the time of the invention to incorporate the DMA controller of Banno into the combination of Abraham, Ishimoto, Koizumi. Their motivation would have been to allow for data transfer to take place without the processor controlling it, thus creating more available processing time.

20. Claims 18-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Ishimoto, Koizumi and Banno as applied to claim 9 above, and in further view of Guttag.

21. With respect to claim 18, Guttag teaches of wherein the data control unit determines whether the data transfer to the user memory space is prohibited or not irrespective of a mode associated with a CPU (column 2, lines 3-54).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi, Banno, and Guttag at the time of the invention to determine the allowability of data transfer independently of the CPU in the combination of Abraham, Ishimoto, Koizumi and Banno as taught in Guttag so that the protection of software is extended against numerous external peripheral devices (Guttag, column 1, lines 65-68).

22. With respect to claim 19, Abraham teaches of wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode (column 2, lines 57-61).

23. Claims 7-8, 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Ishimoto, Koizumi, Banno, and Garney, US patent 5386552.

24. With respect to claim 7, the combination of Abraham, Ishimoto, and Koizumi teach of the limitations cited above with respect to claim 6.

Abraham fails to explicitly teach of delivering an instruction with one or more secure bits into an instruction decoder with a secure bit having a function of determining which of the user memory space and the secure memory space is associated with the instruction under execution.

However, Banno teaches of delivering an instruction with one or more secure bits into an instruction decoder with a secure bit having a function of determining which of the user memory space and the secure memory space is associated with the instruction under execution (column 3, lines 44-51);

Abraham fails to explicitly teach of an interrupt saved information unit a secure bit having a function of adding, upon generation of an interrupt process, the secure bit of the instruction decoder to data saved in a stack area of the built-in RAM space.

However, Garney teaches of a built-in RAM space with a secure bit for receiving and holding the data with one or more secure bits from the general purpose register and delivering the data with secure information held to the general purpose register (column 1, lines 17-40; in the combination in an interrupt processing or context switch, the GPR from the processor of Abraham are saved in the stack of Garney);

an interrupt saved information unit with a secure bit having a function of adding, upon generation of an interrupt process, the secure bit of the instruction decoder to data saved in a stack area of the built-in RAM space (column 1, lines 17-40).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi, and Banno at the time of the invention to identify the memory associated with the requested instruction in the combination of Abraham, Ishimoto, and Koizumi as taught in Banno. Their motivation would have been to prevent a third party from gaining knowledge of the internal program (column 1, lines 20-24).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi, Banno, and Garney at the time of the invention store the processor context upon an interrupt occurrence in the combination as taught in Garney. Their motivation would have been to enable multitasking, thus increasing the efficiency of the processor.

25. With respect to claim 8, the combination of Abraham, Ishimoto, Koizumi, Banno, Garney teach of the limitation cited above with respect to claim 7.

Garney also teaches of a stack pointer for defining a part of the built-in RAM space as the stack area (column 1, lines 25-29; it is abundantly clear to one of ordinary skill in the art that a stack comprises stack pointers which define the stack); and

a saved information rewrite control unit for controlling a rewrite operation in the stack area of the built-in RAM space (column 1, lines 25-29; it is abundantly clear to one of ordinary skill in the art that since data is written to and from the stack, there must be something that controls this);

The combination of Abraham, Ishimoto, Koizumi, Banno, Garney teaches of wherein the saved information rewrite control unit prohibits the rewrite operation if the instruction of the instruction decoder is associated with the user memory space and

intended to rewrite the stack area of the built-in RAM space (since in the combination, writing something that does not originate within the internal memory to an internal memory is inhibited by the protection circuit of Banno, writing state information involving instruction not from the internal memory into an internal RAM stack would not be allowed).

26. With respect to claim 10, the combination of Abraham, Ishimoto, Koizumi, Banno, Garney teach of the limitation cited above with respect to claim 7.

Banno teaches of an operating unit with a secure nit having a function of reflecting the secure bits of the instruction decoder in an arithmetic operation executed in accordance with the instruction decoded by the instruction decoder (column 1, lines 55-65, column 3, lines 44-56).

27. Claims 16-17, 20-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Ishimoto, Koizumi, Banno, and Garney as applied to claim 7 above, and in further view of Guttag.

28. With respect to claims 16 and 20, Guttag teaches of wherein the data control unit determines whether the data transfer to the user memory space is prohibited or not irrespective of a mode associated with a CPU (column 2, lines 3-54).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi, Banno, Garney, and Guttag at the time of the invention to determine the allowability of data transfer independently of the CPU in the combination of Abraham, Ishimoto, Koizumi, Banno, and Garney as taught in Guttag so

that the protection of software is extended against numerous external peripheral devices (Guttag, column 1, lines 65-68).

29. With respect to claims 17 and 21, Abraham teaches of wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode (column 2, lines 57-61).

Allowable Subject Matter

30. Claims 3-5, 11-13 are allowed.

Response to Arguments

31. Applicant's arguments filed 3/14/2008 have been fully considered but they are not persuasive.

32. Applicant argues with respect to the independent claims that the applied art fails to teach of (1) delivering data with **one or more secure bits** into a general purpose register with a secure bit, (2) a built-in RAM space for receiving and holding the data with **one or more secure bits** from the general purpose register, (3) controlling a data transfer to an external space by **using the secure bit**; with the distinction being, "data management by appending secure bits to each data accessed," (applicants remarks 3/14/2008 page 18, lines 3-4) and the applied art limits access based on areas, while the secure bits limit the access in the claims. The examiner disagrees with this reasoning.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the concept of data management by appending secure bits to each data accessed are not recited in the rejected claim(s). The claims merely indicate that the data has one or more secure bits; there is no mention of adding secure bits to the data. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In Abraham as applied to the applicant's claims, the applicant's secure bits are Abraham's addresses (column 2, lines 57-67 and column 3, lines 10-12) which are bits since data takes the form of bits in a computer system.

Conclusion

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL C KROFCHECK/
Examiner, Art Unit 2186

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Michael Krofcheck